



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/035,474	10/25/2001	John E. Barth JR.	FIS920010094US1	5062

32074 7590 03/24/2005

INTERNATIONAL BUSINESS MACHINES CORPORATION
DEPT. 18G
BLDG. 300-482
2070 ROUTE 52
HOPEWELL JUNCTION, NY 12533

EXAMINER

TRIMMINGS, JOHN P

ART UNIT	PAPER NUMBER
----------	--------------

2133

DATE MAILED: 03/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/035,474	BARTH ET AL.	
	Examiner	Art Unit	
	John P Trimmings	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 17 September 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-24 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-24 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 17 July 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

This Office Action is in response to the applicant's amendment dated 9/17/2004.

Claims 1-24 are pending.

Response to Amendment

1. In view of the applicant's changes to the Drawings, the examiner approves the replacement figures 1-3, and withdraws the objection to said drawings.

Response to Arguments

2. Applicant's arguments with respect to claims 1-24 have been considered but are moot in view of the new ground(s) of rejection. The applicant's amendment necessitated new grounds for rejection based on new art (see below).

Claim Rejections - 35 USC § 103

3. Claims 1-5, 13-16 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsumoto et al., U.S. Patent No. 5278839, in view of Lee et al., U.S. Patent No. 5748543, and further in view of Holman et al., U.S. Patent No. 6519735.

As per Claims 1 and 13:

Matsumoto et al. teaches an ECC based circuit and method within an integrated circuit memory for self-repair of a failed memory element therein (column 1 lines 53-56), comprising: automatically identifying and recording locations of memory failures (column 4 lines 67-68 and column 5 lines 1-29) within said integrated circuit memory by

Art Unit: 2133

processing data bits retrieved from addressed memory locations of said integrated circuit memory of the integrated circuit (FIG.1 30 and column 8 lines 52-67 and column 13 lines 33-40); whereby said failed memory element is identified and repaired automatically by circuitry within said integrated circuit (column 7 lines 37 to column 8 line 5), replacing failed elements (column 5 lines 14-29). Mut Matsumoto fails to teach basing repairs on pattern, and identifying failure based on check bits. But, Lee et al., in the Abstract and in column 3 lines 31-43 teaches using logic circuits within the integrated circuit to automatically identify failure patterns based on said locations (defect indicating signal); and using at least second logic circuits within said integrated circuit (spare substituting circuit) to automatically replace a failed memory element with a redundancy element based on at least one said identified failure pattern. It would have been obvious to additionally modify the circuit and method of Matsumoto et al. by adding the failure replacement units taught by Lee et al. into the circuit, because Lee et al., in column 2 lines 27-33, also boasts the advantage of repair after device packaging. One with ordinary skill in the art at the time of the invention, motivated as suggested above for Lee et al., would combine the systems in order to have post manufacture testing and repair capabilities. But neither Matsumoto et al. nor Lee et al. teach identification of bit failure while reading out of a memory utilizing ECC. But in an analogous art, Holman et al. does teach this feature (see Abstract and FIG.1 and column 1 lines 56-67 and column 2 lines 1-7, where the location of a defective cell in a memory is provided by an ECC means. And in column 1 lines 48-54, the advantage is a better method of locating a defective memory cell prior to isolating the failed bit. One

with ordinary skill in the art, motivated as suggested, would have found it obvious to use the compact bit failure system of Holman et al. to located failures in a self-repairing device such as in Matsumoto et al. and Lee et al.

As per Claims 2 and 14:

The method and circuit of claims 1 and 13 wherein said integrated circuit memory is of the type selected from dynamic random access memory (DRAM), static random access memory (SRAM), and electrically erasable programmable read only memory (EEPROM) including flash memory is also taught by Matsumoto et al. in column 1 lines 6-16.

As per Claims 3 and 24:

The method and circuit of claims 1 and 13 wherein said failed memory element is replaced with a redundancy element selected from the group consisting of at least row redundancy element and column redundancy element is further taught by Lee et al. in the Abstract.

As per Claims 4, 5, 15 and 16:

Based on the method and circuit of claims 1 and 13 wherein said electrically alterable circuit connections include at least one selected from the group consisting of electronic fuse and electronic anti-fuse is also taught by Lee et al. in the Abstract.

4. Claims 10 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsumoto et al., U.S. Patent No. 5278839, in view of Lee et al., U.S. Patent No. 5748543, and further in view of Holman et al., U.S. Patent No. 6519735 as applied to Claims 2 and 14, and further in view of Hughes et al., U.S. Patent No. 6691252. The

method and circuit of claims 2 and 14 wherein said integrated circuit memory is incorporated within an integrated circuit having a microprocessor is taught by Hughes et al. in column 9 lines 59-65. It would have been obvious to modify the circuit of Matsumoto et al. to additionally provide failure recovery to embedded memories within a microprocessor. And Hughes et al., in column 3 lines 55-59 recites an advantage being the capability to repair a fault at the same time testing continues to be executed within the circuit. One with ordinary skill in the art at the time of the invention, motivated by Hughes et al. as suggested, would combine the references in order to simultaneously repair while operating the system, and so the claims are rejected.

5. Claims 11-12 and 22-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsumoto et al., U.S. Patent No. 5278839, in view of Lee et al., U.S. Patent No. 5748543 and further in view of Holman et al., U.S. Patent No. 6519735 as applied to Claims 2 and 14, and in view of Hughes et al., U.S. Patent No. 6691252 as applied to Claims 10 and 21 above, and further in view of Eaton et al., U.S. Patent No. 4939694.

As per Claims 11 and 22:

The method and circuit of claims 10 and 21 wherein said integrated circuit memory is of the DRAM type and wherein said locations are automatically recorded while said integrated circuit is in a normal operational mode is further taught by Eaton et al. in column 1 lines 15-16 and column 7 lines 1-28. It would have been obvious to modify the circuit and method of Matsumoto et al. to include DRAM type memories and testing to occur under normal conditions thereby reducing cost. And in column 2 lines

Art Unit: 2133

14-17, Eaton et al. recites the advantage of less costly testing expense as well as improved product yield. And one with ordinary skill in the art at the time of the invention, motivated by Eaton et al., would combine the references to reduce cost, and so the claims are rejected.

As per Claims 12 and 23:

The method and circuit of claims 11 and 22 wherein said failed memory element is automatically replaced when said integrated circuit remains installed within a product for normal use is also taught by Eaton et al. in column 7 lines 43-55. And in view of the motivation above, the claims are rejected.

6. Claims 6, 8, 9 and 17, 19, 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsumoto et al., U.S. Patent No. 5278839, in view of Lee et al., U.S. Patent No. 5748543, and further in view of Holman et al., U.S. Patent No. 6519735 as applied to Claims 1 and 13 above, and further in view of Eaton et al., U.S. Patent No. 4939694.

As per Claims 6 and 17:

References Matsumoto et al., Lee et al. and Holman et al., fail to further teach the method and circuit of claims 1 and 13 wherein said memory failures are automatically recorded, said failure patterns automatically identified, and said failed memory element is automatically replaced while said integrated circuit is in a normal operational mode. In an analogous art however, Eaton et al. does teach this feature in column 7 lines 1-28. It would have been obvious to modify the circuit and method of Matsumoto et al. to include DRAM type memories and testing to occur under normal

Art Unit: 2133

conditions thereby reducing cost. And in column 2 lines 14-17, Eaton et al. recites the advantage of less costly testing expense as well as improved product yield. And one with ordinary skill in the art at the time of the invention, motivated by Eaton et al., would combine the references to reduce cost, and so the claims are rejected.

As per Claims 8 and 19:

References Matsumoto et al., Lee et al. and Holman et al. fail to further teach the method and circuit of claims 1 and 13 wherein said locations are automatically recorded while said integrated circuit is in a normal operational mode and wherein said failed memory element is automatically replaced only during a non-normal operational mode of said integrated circuit. Eaton et al. does further teach this optional mode in column 10 lines 11-32. And in view of the motivation previously cited for Eaton et al., the claims are rejected.

As per Claims 9 and 20:

Eaton et al. also teaches the method and circuit of claims 8 and 19 wherein said non-normal operational mode is of a type selected from power-up mode or power-down mode (column 7 lines 38-43). And in view of the motivation previously cited for Eaton et al., the claims are rejected.

7. Claims 7 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsumoto et al., U.S. Patent No. 5278839, and in view of Lee et al., U.S. Patent No. 5748543, and further in view of Holman et al., U.S. Patent No. 6519735 as applied to Claims 1 and 13 above, and in view of Eaton et al., U.S. Patent No. 4939694 as applied to Claims 6 and 17 above, and further in view of Hotaka, U.S. Patent No. 6442083.

Art Unit: 2133

Hotaka further teaches the method and circuit of claims 6 and 17 wherein said memory asserts a busy signal during the time that said memory is unavailable for access during which at least one operation is being performed from the group consisting of: identifying said failure patterns and replacing said failed memory element (column 3 lines 65-67, column 4 lines 1-16 and column 6 lines 21-28. It would have been obvious to modify the circuit and method of Matsumoto et al. to assert a busy signal, to an attached microprocessor in one case, when the repair circuit is busy in order to preclude possible conflicts, and to locate repair cells close to the failures for fast repair. And in column 1 lines 53-67 and column 2 lines 1-15 recited the advantage of location redundant cells within the main memory area to reduce chip size, and accommodate repair (speed up repair). And one with ordinary skill in the art at the time of the invention, motivated by Hotaka to reduce chip size, would combine references, and so the claims are rejected.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the

Art Unit: 2133

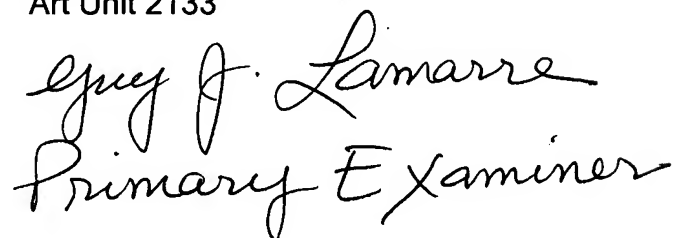
shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John P Trimmings whose telephone number is 703-305-0714. The examiner can normally be reached on Monday through Thursday, 7:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on 703-305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).


John P Trimmings
Examiner
Art Unit 2133


Primary Examiner

jpt